UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/622,923	07/17/2003	Gregg Baeckler	015114-066500US	2777

26059 7590 11/02/2005

TOWNSEND AND TOWNSEND AND CREW LLP/ 015114
TWO EMBARCADERO CENTER
8TH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
PARIHAR, SUCHIN	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/622,923	BAECKLER ET AL.	
	Examiner	Art Unit	
	Suchin Parihar	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☒ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This application 10/622,923 has been examined. Claims 1-22 are pending

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 314 in Figure 3. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

1. Claims 7,8,13,15,20 and 22 are objected to because of the following informalities: the claims listed above fail to specifically define the terms or symbols N and M. Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1, 7, 8-10, 12-14, and 20-22 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Betz et al. (6,957,412) in view of Kelsey et al. (5,452,227).

4. With respect to claim 1, Betz teaches a method for the design of a programmable integrated circuit (Col 1, lines 60-67, i.e. design ... on a programmable integrated circuit) wherein a first and second LUT are selected from the design (Col 1, lines 38-40, i.e. first logic element, second logic element), and the first and second LUT's are combined into one circuit element (Col 1, lines 11-13, i.e. combining functional blocks into fewer programmable circuit elements). Betz fails to teach a method that determines whether first and second LUT implement the same function. However, Kelsey teaches a method related to a programmable logic device wherein it is determined whether first and second LUT implement the same function, and if so, both LUT's are combined into a shared circuit element (Col 2, lines 30-35, i.e. reduce redundant logic). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Kelsey into the method of Betz because Kelsey suggests that such redundant logic reduction is necessary in the design of a PLD-related device (Col 2, lines 20-44).

5. With respect to claim 7, Betz in view of Kelsey teaches all the elements of claim 1, from which the claim depends, wherein. Betz teaches a method for the design of a programmable integrated circuit (Col 1, lines 60-67, i.e. design ... on a programmable integrated circuit) wherein determining whether LUTs have at least some number (N) common input signals (Col 2, lines 13-17, i.e. user-specified constraint), if the LUTs do

not have at least some number (N) of common input signals (Col 8, lines 15-21, i.e. violating user-specified constraint), preventing the masks of the LUTs from being combined (Col 8, lines 21-25, i.e. prevent some combinations of functional blocks).

6. With respect to claim 8, Betz in view of Kelsey teaches all the elements of claim 7, from which the claim depends, wherein. Betz teaches a method for the design of a programmable integrated circuit (Col 1, lines 60-67, i.e. design ... on a programmable integrated circuit) wherein determining whether LUTs have more than some number (M) of unique input signals (Col 2, lines 13-17, i.e. user-specified constraint), if the LUTs have more than some number (M) of unique input signals (Col 8, lines 15-21, i.e. violating user-specified constraint), preventing the masks of the LUTs from being combined (Col 8, lines 21-25, i.e. prevent some combinations of functional blocks).

7. With respect to claim 9, Betz in view of Kelsey teaches all the elements of claim 1, from which the claim depends, wherein. Kelsey teaches a method wherein determining if both the LUTs both perform the same function further comprises determining if an output value of the first LUT equals an output value of the second LUT for each possible input value that is applied to the input terminals of both of the LUTs (Col 2, lines 35-44, i.e. simulation and behavioral model produce identical outputs).

8. With respect to claim 10, Betz in view of Kelsey teaches all the elements of claim 1, from which the claim depends, wherein. Betz teaches a method for the design of a programmable logic device where a third and fourth LUT are selected from a design (Col 3, lines 64-66, i.e. other circuit combinations). Kelsey teaches a method related to a programmable logic device wherein it is determined whether third and fourth LUT

implement the same function, and if so, both LUT's are combined into a shared circuit element or mask (Col 2, lines 30-35, i.e. reduce redundant logic).

9. With respect to claim 12, Betz in view of Kelsey teaches all the elements of claim 1, from which the claim depends, wherein. Betz teaches a method for the design of a programmable logic device comprising breaking apart the mask of the LUTs if the mask lies in a critical path (Col 6, lines 38-50, i.e. time critical path: low criticality, high criticality) in the design, and placing the first and second LUTs into different logic elements within the design (Col 2, lines 14-17, i.e. if selected combination is feasible in light of electrical an user-specified constraints [critical path], the combination is performed).

10. With respect to claim 13, Betz in view of Kelsey teaches all the elements of claim 1, from which the claim depends, wherein. Betz teaches a method for the design of a programmable integrated circuit (Col 1, lines 60-67, i.e. design ... on a programmable integrated circuit) comprising: after determining whether both LUTs implement the same function, determining if LUTs have at least some number N common input signals, and no more than M unique input signals (Col 2, lines 10-17, i.e. user-specified constraint), wherein LUT masks are combined into the shared LUT mask only if the LUTs have at least N common and no more than M unique input signals (Col 2, lines 12-17, i.e. if the combination is feasible in light of user-specified constraints, the combination is performed).

11. With respect to claim 14, Betz teaches a computer system (Col 3, lines 15-20, i.e. CAD system) that combines LUTs in a design for a programmable integrated circuit

(Col 1, lines 60-67, i.e. design ... on a programmable integrated circuit) wherein the system comprising: code for selecting first and second LUT's in the design (Col 1, lines 38-40, i.e. first logic element, second logic element), and code for combining masks of the LUT's in the design if the LUTs generate the same function (Col 1, lines 11-13, i.e. combining functional blocks into fewer programmable circuit elements). Betz fails to teach a computer system that provides code to determine whether first and second LUT implement the same function. However, Kelsey teaches a computer system (Col 3, lines 10-12, i.e. Computer Aided Engineering Tool) related to a programmable logic device wherein code is provided for determining whether first and second LUT implement the same function, and if so, both LUT's are combined into a shared circuit element (Col 2, lines 30-35, i.e. reduce redundant logic). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Kelsey into the computer system of Betz because Kelsey suggests that such redundant logic reduction is necessary in the design of a PLD related device (Col 2, lines 20-44).

12. With respect to claim 20, Betz in view of Kelsey teaches all the elements of claim 14, from which the claim depends, wherein. Betz teaches a computer system wherein the code is provided to determine if the LUTs have at least N common and no more than M unique input signals (Col 2, lines 10-17, i.e. user-specified constraint in lieu of CAD Tool) wherein implementation of the code for comparing the output values of the first and second LUTs is prevented if the first and second LUTs have less than N common input signals or more than M unique input signals (Col 8, lines 12-15, i.e. a combination is feasible if it does not violate any user-specified constraints).

13. With respect to claim 21, Betz in view of Kelsey teaches all the elements of claim 14, from which the claim depends, wherein. Betz teaches a computer system (Col 3, lines 15-20, i.e. computer-aided design system) for the design of a programmable logic device wherein the code is provided for breaking apart the mask of the LUTs if the mask lies in a critical path (Col 6, lines 38-50, i.e. time critical path: low criticality, high criticality) in the design, and placing the first and second LUTs into different logic elements within the design (Col 2, lines 14-17, i.e. if selected combination is feasible in light of electrical an user-specified constraints [critical path], the combination is performed).

14. With respect to claim 22, Betz in view of Kelsey teaches all the elements of claim 18, from which the claim depends, wherein. Betz teaches a computer system wherein the code is provide for determining if the LUTs have at least N common and no more than M unique input signals after the output values of the LUTs have been compared (Col 8, lines 8-13, i.e. user-specified constraints in lieu of CAD Tool) and the masks of the first and second LUTs are not combined if the LUTs have less than N common or more than M unique input signals (Col 8, lines 20-25, i.e. an electrical rule may also prevent some combinations of functional blocks).

15. **Claims 2-6, 11, and 15-19 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Betz et al. (6,957,412) in view of Kelsey et al. (5,452,227) and further in view of Andreev et al. (6,848,094). With respect to claims 2-6, 11, and 15-19, Betz in view of Kelsey teaches all the elements of claim 1 from which claims 2-6 and 11 depend, and also teaches all the elements of claim 14, from which claims 15-19

depend, wherein. Betz in view of Kelsey fails to specifically teach a method/system wherein input signals are rearranged iteratively in order to determine whether two LUTs implement the same function. However, Andreev teaches a method of determining whether two LUTs implement the same function (Col 1, lines 5-12) wherein the order of input signals the LUTs are rearranged in order to determine whether both LUTs implement the same function (Col 1, lines 20-34). It would have been obvious to one of ordinary skill in the art to incorporate Andreev into the method of Betz and Kelsey because Andreev suggests that the re-ordering of inputs and corresponding outputs is helpful in removing redundant circuits, i.e. determining whether two LUTs implement the same function (Col 1, lines 20-35).

16. With respect to claim 2, Betz in view of Kelsey teaches all the elements of claim 1, from which the claim depends, wherein. Andreev teaches a method of determining whether two LUTs implement the same function (Col 1, lines 5-12) wherein common input signals of LUTs are identified, and the order of input signals of one of the LUTs are rearranged so that the common input signals are applied to a corresponding input terminal in both of the LUTs, and this method determines whether both LUTs implement the same function based on the first rearranged order of input signals (Col 1, lines 20-34).

17. With respect to claim 3, Betz in view of Kelsey and Andreev teaches all the elements of claim 2, from which the claim depends, wherein. Andreev teaches a method of determining whether two LUTs implement the same function (Col 1, lines 5-12) wherein the order of at least two uncommon input signals of one of the LUTs are

rearranged with respect to the input terminals of that LUT, and this method determines whether both LUTs implement the same function (Col 1, lines 20-34).

18. With respect to claim 4, Betz in view of Kelsey teaches all the elements of claim 1, from which the claim depends, wherein. Andreev teaches a method of determining whether two LUTs implement the same function (Col 1, lines 5-12) wherein the order of at least two input signals of one of the LUTs are rearranged with respect to the input terminals of that LUT, and this method determines whether both LUTs implement the same function (Col 1, lines 20-34).

19. With respect to claim 5, Betz in view of Kelsey and Andreev teaches all the elements of claim 4, from which the claim depends wherein. Betz teaches a method for the design of a programmable integrated circuit (Col 1, lines 60-67, i.e. design ... on a programmable integrated circuit) wherein a first and second LUT are combined into a shared LUT mask (Col 1, lines 11-13, i.e. combining functional blocks into fewer programmable circuit elements). Andreev teaches a method of determining whether two LUTs implement the same function (Col 1, lines 5-12) wherein the order of at least two input signals of one of the LUT's are rearranged with respect to the input terminals of that LUT, and this method determines whether both LUTs implement the same function (Col 1, lines 20-34).

20. With respect to claim 6, Betz in view of Kelsey and Andreev teaches all the elements of claim 5, from which the claim depends, wherein. Andreev teaches a method for determining whether two LUTs implement the same function (Col 1, lines 5-12). Betz teaches a method wherein two LUTs are combined into a shared mask (Col

1, lines 11-13, i.e. combining functional blocks into fewer programmable circuit elements) if it is determined that the LUTs are combinable (i.e. implement same function, as suggested by Andreev: Col 1, lines 7-10). Andreev also teaches rearranging the order of at least two input signals of the first LUT with respect to the input terminals of that LUT because it has not yet been determined that the LUT's implement the same function.

21. With respect to claim 11, Betz in view of Kelsey teaches all the elements of claim 10, from which the claim depends, wherein. Andreev teaches a method of determining whether two LUTs implement the same function (Col 1, lines 5-12) wherein the order of at least two input signals of one of the LUTs are rearranged with respect to the input terminals of that LUT if previous rearrangements of input signals to not determine same function (Col 1, lines 20-34).

22. With respect to claim 15, Betz in view of Kelsey teaches all the elements of claim 14, from which the claim depends, wherein. Andreev teaches a computer system wherein at least some number N of common input signals for the first and second LUT are determined, and the order of input signals of one of the LUTs are rearranged so that the common input signals are applied to a corresponding input terminal in both of the LUTs, in the same order, to provide a first rearranged order, and this method determines whether both LUTs implement the same function (Col 1, lines 20-34).

23. With respect to claim 16, Betz in view of Kelsey teaches all the elements of claim 15, from which the claim depends, wherein. Andreev teaches a computer system wherein the code is provided for rearranging an order of al least two uncommon input

signals with respect to input terminals of one of the LUTs to provide a second rearranged order, if the LUTs do not implement the same function (Col 1, lines 20-34). Kelsey teaches a computer system (Col 3, lines 10-12, i.e. Computer Aided Engineering Tool) which includes code to compare output values of the LUTs to determine if the LUTs generate the identical function based on the second rearranged order of the input signals (Col 2, lines 28-33).

24. With respect to claim 17, Betz in view of Kelsey teaches all the elements of claim 14, from which the claim depends, wherein. Andreev teaches a computer system (Col 7, lines 57-60, i.e. computer program of the present invention) wherein code is provided to determine whether two LUTs implement the same function (Col 1, lines 5-12) which involves the rearrangement of the order of at least two input signals of one of the LUTs with respect to the input terminals of that LUT (Col 1, lines 20-34).

25. With respect to claim 18, Betz in view of Kelsey and Andreev teaches all the elements of claim 17, from which the claim depends, wherein. Andreev teaches a computer system (Col 7, lines 57-60, i.e. computer program of the present invention) wherein code is provided for combining masks of the LUTs (Col 1, lines 10-12, i.e. removing redundant circuits) in the design if the LUTs implement the identical function with the first rearranged order (Col 1, lines 23-25, i.e. re-ordering inputs), and code for rearranging the order of input signals of the LUTs with respect to the input terminals of that LUT to provide a second rearranged order of the input signals, if the LUTs do not implement the identical function with the first rearranged order (Col 1, lines 20-34)).

26. With respect to claim 19, Betz in view of Kelsey and Andreev teaches all the elements of claim 18, from which the claim depends, wherein. Andreev teaches a computer system (Col 7, lines 57-60, i.e. computer program of the present invention) wherein code is provided for combining masks of the LUTs (Col 1, lines 10-12, i.e. removing redundant circuits) in the design if the LUTs implement the identical function with the second rearranged order (Col 1, lines 23-25, i.e. re-ordering inputs), and code for rearranging the order of input signals of the LUTs with respect to the input terminals of that LUT to provide a third rearranged order of the input signals, if the LUTs do not implement the identical function with the second rearranged order (Col 1, lines 20-34)).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suchin Parihar whose telephone number is 571-272-6210. The examiner can normally be reached on Mon-Fri, 7:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached at 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Suchin Parihar

Suchin Parihar
Examiner
AU 2825

A. M. Thompson
Primary Examiner
Technology Center 2800